METHOD AND APPARATUS FOR POWERING DOWN THE CPU/MEMORY CONTROLLER COMPLEX WHILE PRESERVING THE SELF REFRESH STATE OF MEMORY IN THE SYSTEM

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ABSTRACT OF THE DISCLOSURE

Power management logic maintains memory in a computer system in the self refresh state during a power savings state in which power is removed from the memory controller. A memory control circuit, separate from the power management logic, controls the memory during other operational modes. The power management logic maintains the system memory in the self refresh state by driving memory control signal(s) at appropriate values during the power savings state.